AMENDMENTS TO THE SPECIFICATION

Please replace the title with the following amended title:

STACKED SEMICONDUCTOR PACKAGE WITH MULTIPLE CHIPS MOUNTED TO A SINGLE SUBSTRATE

Please replace the paragraph bridging pages 8 and 9 with the following amended paragraph:

A semiconductor chip with the packaged structure, for example, is disclosed in Japanese Patent Application Publication (JP-A) No. H11-135562 and is also disclosed in Japanese Patent Application Publication (JP-A) No. H11-186449. The semiconductor chip has structure as illustrated in Fig. 5 or 6. In Fig. 5 or 6, the semiconductor chip is manufactured by mounting an elemental chip 202 or 302 on a ~~substrate 202~~substrate 201 or 301, electrically connecting wires (pads) 203 or 303 of the elemental chip 202 or 302 to wires 204 or 304 on the substrate by means of wire bonding 205 or 305 (or inner lead bonding, flip-chip connection, and so on), and ~~encupsulating~~ encapsulating the elemental chip 202 or 302 and the substrate in a resin mold 207 or 307 to protect a conductive pattern 206 or 306 on the substrate.

Please replace the first full paragraph on page 9 with the following amended paragraph:

Alternatively, there is a semiconductor chip with another packaged structure obtained according to a method in which a packaging process (post-process) is integrated with the wafer process (pre-process) and the packaging process is completed at a wafer level. The

semiconductor chip is referred to as a wafer level CSP (Chip Size Package or Chip Scale Package) or a wafer process package. For example, the semiconductor chip of the type is disclosed in Japanese Patent Application Publication (JP-A) No. 2002-261192 and is also disclosed in Japanese Patent Application Publication (JP-A) No. 2003-298005. As illustrated in Fig. 7, the semiconductor chip disclosed in the former document is structured by forming a protection film 402, a rewiring layer 403, a copper post 404 and the like on a semiconductor substrate 401 which undergo a wafer process, and encapsulating them in a resin mold 405.

Please replace the third full paragraph on page 18 with the following amended paragraph:

Referring to Fig. 21A, the ground plane and/or the power supply plane (flat ~~wirng~~wiring) forming the transmission line may comprise a plurality of ground plane parts and/or power supply wiring plane parts (plates) 91, 92.